MOS-GATED TRANSISTOR WITH IMPROVED UIS CAPABILITY

ABSTRACT OF THE DISCLOSURE

In accordance with the present invention, a transistor includes a semiconductor substrate forming a collector region. A drift region of a first conductivity type extends over the semiconductor substrate. First and second well regions of a second conductivity each extends from an upper surface of the drift region into and terminates within the drift region. The first well region is coupled to an emitter terminal while the second well region floats. The first and second well regions are separated by an impurity region of the first conductivity type such that each of the first and second well regions forms a separate pn junction with the impurity region.

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